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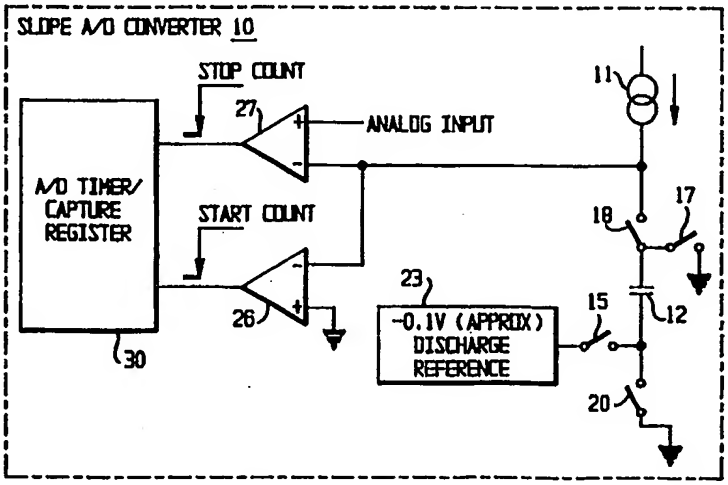

(57) Abstract

A slope analog-to-digital converter (10) performs a conversion of the instantaneous value of a variable analog input voltage to a digital value with reduced conversion errors by starting the ramp charging prior to initiation of the counter/time/register (30). The charging capacitor (12) is first discharged to a level slightly below analog ground by a discharge reference circuit (23). The charging source (11) is then connected to the capacitor (12) to initiate the ramp voltage. When the ramp voltage passes through the ground level reference as sensed by a start count comparator (26) accumulation of counting pulses is begun. The capacitor voltage is ramped up until the level of the ramp voltage exceeds that of the analog input as sensed by a stop count comparator (27). The accumulated count constitutes a digital value corresponding to the value of the analog input. After the cumulative count is obtained the capacitor is again discharged to a level below ground in preparation for the next conversion.

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SLOPE ANALOG-TO-DIGITAL CONVERTER WITH RAMP INITIATED PRIOR TO COUNTER

Background of the Invention

The present invention relates generally to analog-to-digital (A/D) converter devices, and more particularly to slope A/D converters which are especially suitable for use in conjunction with microcontrollers.

Microcontrollers are microprocessors which are specially implemented with primary and peripheral functions and capabilities to enable control of certain specified parameters of an external system. In performing these functions, it is frequently necessary to detect when a controlled parameter has reached a certain value relative to a predetermined maximum or minimum value. For example, the controlled parameter may be the temperature within an enclosure such as a room, or an oven. In any event, the controlled parameter is generally of analog form and is converted to an electrical signal by means of an appropriate transducer -- a thermoelectric transducer such as a thermistor in the case of temperature. For purposes of analysis and use by the microcontroller in its control functions, however, it is necessary to convert the analog signal to digital form. Typically, this is done by means of an A/D converter.

One type of such a converter is a slope A/D converter. In its simplest form, the slope A/D converter operates by starting a timer at time (t) = 0, which then commences counting at a predetermined fixed frequency while a capacitor in the converter circuit is being charged by a constant current source. At the moment that the capacitor reaches a charge (i.e., is charged) to a voltage that just exceeds the

unknown sampled analog input voltage to the circuit, a comparator having the unknown input voltage and the capacitor voltage as inputs changes state, to cause the timer to stop counting. The digital (converted) value of the sampled input voltage is represented by the count of the timer from the moment of time that the charging of the capacitor began (at t = 0), up to the moment of time that the comparator changed state.

Such a calculation or determination of the value of the unknown sampled analog input voltage is actually only an approximation, because it assumes that at time t = 0, at which the timer count is zero, the voltage on the capacitor was zero. This assumption is frequently erroneous. One significant reason for the error is a delay in the time the charging of the capacitor commences, attributable to the "turn-on" time of the constant current source. Another significant but more subtle reason is that a residual voltage usually remains on the capacitor from the previous or even earlier charging cycle because of dielectric absorption inherent in the capacitor, despite the fact that the capacitor is short-circuited to ground before each new charging cycle (i.e., each new A/D conversion) is commenced. These factors lead to errors in the starting time of the count and in the time at which the capacitor charge reaches the instantaneous voltage of the analog input (and, thus, the ending time of the count), resulting in conversion errors.

In at least one previously-available slope A/D converter, slope reference voltages are incorporated in an attempt to improve the conversion accuracy. In that instance, a pair of reference voltages is included in the circuit, one high (S_{REFHI}) and the other low (S_{REFLO}), for calculating the actual slope of the charging capacitor

voltage. By knowing the actual slope, its intercept with the X-axis can be determined for use in a correction of the conversion value. In particular, the X-intercept corresponds to the count when the voltage across the capacitor is zero (as an offset), and this value may be used to compensate for the subsequent A/D conversion results.

But this method has certain drawbacks. First, the hardware needed for an adequate circuit must include means for generating the two slope reference voltages, as well as for obtaining the ratio $S_{REFLO}/(S_{REFHI} - S_{REFLO})$, which is critical to the determination, and for calibration of the ratio and maintaining it constant to attain the necessary accuracy. This requirement of additional hardware for generating the references, as well as the circuitry and calibration apparatus to accommodate precise operation, can add considerable expense to the device and thus adversely affect its competitiveness.

Another disadvantage of this prior technique is that the slope references must be converted separately from the analog input, which reduces the accuracy of the conversion and decreases the throughput of the conversion process. Since optimizing the speed of the calculation is preeminent, the slope of the capacitor voltage should be calculated only periodically, rather than with each conversion of the input signal. But conversion errors arise in part because of a desire for rapid conversion, which is frustrated by often-repeated slope calculations.

The dielectric absorption of the capacitor is a function of the initial voltage across the capacitor. The amount of time required to complete discharge the capacitor must be adjusted according to this initial capacitor voltage. Two adjacent

(i.e., successive) conversion cycles typically involve analog input signals of different magnitude. The first conversion cycle charges the capacitor to a certain voltage which should be substantially identical to that of the analog input -- say, 1 volt, for the sake of example -- to cause the timer to stop its count, and the capacitor is then discharged in preparation for the next conversion cycle. The second conversion cycle then charges the capacitor to, say, an analog input signal value of 3 volts, which again stops the timer count, and initiates another discharge of the capacitor. If both of these conversion cycles have the same discharge time, the value of the residual charge on the capacitor upon completion of the discharge portion of the cycle will not be the same at the commencement of the next respective conversion cycle, resulting in errors in the two (or more) analog-to-digital conversions. That is, the slope calculation is inaccurate from conversion cycle to conversion cycle.

To minimize such errors, the capacitor should be discharged to the same residual voltage at the end of each conversion cycle (actually, $\geq V_{REF}$, where V_{REF} is positive reference potential), and the slope should be re-calculated for each conversion. But this means a slowing of the conversion throughput, which is disadvantageous for reasons mentioned above.

Another drawback of calculations using reference voltages S_{REFHI} and S_{REFLO} is that considerable mathematical manipulation must be performed to arrive at an offset count (C_{OFFSET}). Referring to the Cartesian coordinate X-Y plot of **FIG. 1**, the equation for a line is $y = mx + b$, where y is the value measured along the Y-axis, x is the value measured along the X-axis, m is a multiplier, and b is a constant representative of the displacement of the value y from the origin (0) along the Y-

axis. In the instant situation, however, the equation for determining the X-intercept (C_{OFFSET}) is more complex, albeit of the same form, as follows:

$$C_{OFFSET} = C_{REFLO} - K_{REF} (C_{REFHI} - C_{REFLO}), \quad (1)$$

where C_{OFFSET} is the offset count (X-intercept), K_{REF} is the ratio $S_{REFLO}/(S_{REFHI} - S_{REFLO})$, and C_{REFHI} and C_{REFLO} are the A/D conversion results (in counts) for S_{REFHI} and S_{REFLO}. Subsequently, the sampled input voltage V_{IN} is calculated as:

$$V_{IN} = (C_{IN} - C_{OFFSET}) \cdot K_{BG}/(C_{BG} - C_{OFFSET}), \quad (2)$$

where C_{IN} is the input count, K_{BG} is the bandgap voltage, and C_{BG} is the bandgap voltage count.

It should be apparent from equations (1) and (2) that implementing a determination of slope voltage becomes quite unwieldy, especially when using assembly language, as is typically the case with a microcontroller. The ideal slope, shown by the solid line on the plot, is equal to $\Delta V/\Delta t = I/C$ (where I is a constant current), while the dashed line indicates the actual same slope with slope displacement attributable to dielectric absorption. This corresponds to non-zero X and Y intercepts. The X-intercept is the offset count (C_{OFFSET}) that must be used to adjust the analog input count value as shown by equations (1) and (2). In an implementation of a slope A/D conversion for determining the input voltage according to the prior art of **FIG. 1**, then, the conversion and solving of resulting equations require substantial program memory and consume a significant number of computation cycles.

Accordingly, it is a principal aim of the present invention to provide a new and improved slope A/D converter, which is of relatively simple configuration

and which reduces the conversion errors encountered with slope A/D converters of the prior art.

Summary of the Invention

In a preferred embodiment of the invention, an enhanced slope A/D converter uses two references, one of which is a positive voltage indicative of a predetermined bandgap voltage, nominally 1.20V, equal to the positive reference potential, and the other of which is analog ground. The second reference is actually a sample of the instantaneous level of the analog input signal to the second comparator, with respect to analog ground acting as the comparator reference input.

A capacitor in the slope A/D converter is charged via a switching circuit to a first imprecise voltage level which is slightly below the level of electrical ground. The capacitor is then charged by a constant current source to a second voltage level which is above ground and is predetermined to be higher than any sample of the instantaneous level of an analog input signal to be converted to a digital value. A first comparator is responsive to the capacitor reaching a level of charge just exceeding ground level, to trigger commencement of a timed count by a timer/register. A second comparator is responsive to the capacitor reaching a charge level representative of the analog input voltage which exceeds ground level but is normally less than or equal to the bandgap voltage, to trigger a cessation of the timed count. The register portion of the timer/register stores the digital conversion value equivalent to the count reached upon cessation, which is representative of the digital value of the instantaneous level of the sampled analog

input signal. The capacitor is then discharged to intialize the converter for the next analog-to-digital conversion.

Such a slope A/D converter is not as susceptible to conversion errors attributable to the turn-on delay of the constant current source, because the source is already operating -- having charged the capacitor from the below-ground level up to ground level before the count is commenced --; or attributable to a residual charge on the capacitor, because any such charge is immaterial to either the commencement or cessation of the count since those points are determined by the capacitor voltage reaching ground level and reaching the instantaneous level of the sampled analog input signal.

Accordingly, it is a more specific objective of the present invention to provide a slope A/D converter with substantial improvement in conversion accuracy by avoiding a delay in operation of the charging means for the measuring capacitor, and by eliminating the effect of a residual charge on the capacitor between conversions.

Yet another aim of the invention is to provide a microcontroller for use with a slope A/D converter to control the value of a parameter which is applied as a representative input to the converter.

Brief Description of the Drawings

The above and still further aims, objectives, features, aspects and attendant advantages of the present invention will become apparent from a consideration of the following detailed description of a presently contemplated best mode of practicing the invention, by reference to a preferred embodiment and method thereof, taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a plot of a plane Cartesian coordinate system wherein positions of points are determined from abscissa and ordinate parallel to X- and Y-axes, respectively, for explanation of a prior art X-intercept calculation of slope A/D conversion, described above;

FIG. 2 is a block diagram of a preferred embodiment of a slope A/D converter according to the present invention;

FIG. 3 is a graph illustrating the operation of the converter of **FIG. 2**;

FIG. 4 is a more detailed schematic diagram of the slope A/D converter of **FIG. 2**;

FIG. 5 is a plot of a plane Cartesian coordinate system similar to that of **FIG. 1**, but illustrating the improved effect obtained with the device and method of the present invention;

FIG. 6 is an alternative embodiment of the slope A/D converter of **FIG. 2**; and

FIG. 7 is a simplified block diagram showing a slope A/D converter in conjunction with a microcontroller according to the invention.

Detailed Description of the Presently Preferred Embodiment and Method

A preferred embodiment of a slope A/D converter **10** according to the present invention is shown in block diagrammatic form in **FIG. 2**. The circuit **10** includes a constant current source **11**, a capacitor **12**, a plurality of switches (which may be transistors or other electronic devices, despite the conventional schematic single-throw representation in the Figure) **15**, **17**, **18**, and **20**, a discharge reference voltage source **23**, a pair of comparators **26** and **27**, and an A/D timer and capture register (sometimes referred to herein as a counter/timer) **30**.

Constant current source **11** has an output port connected to one pole of switch **18**, to a first (negative) input of comparator **26**, and to a first (negative) input of comparator **27**. The arm of switch **18** is connected to the arm of switch **17**, the latter having a pole connected to electrical ground. It will be understood that each the switches may be and preferably is a metal-oxide-silicon field effect transistor (MOSFET) with source, drain, and gate electrodes, and an electrical path which is open or closed through the source-drain electrodes depending on the relative voltages on those and the gate electrode. The arms of switches **17** and **18**, in addition to being connected to each other, are connected to one terminal (plate) of capacitor **12**. The other terminal of the capacitor is connected to a pole of switch **15** and a pole of switch **20**. The arm of switch **15** is connected to discharge reference voltage source **23**, and the arm of switch **20** is connected to ground.

The second (positive) input of comparator **26** is connected to ground, and the second (positive) input of comparator **27** is connected to receive the analog input signal whose instantaneous value has been sampled (for example, by a sample-

and-hold circuit, not shown) and is to be converted to a digital value by the converter circuit **10**. The outputs of the two comparators are coupled to respective start (commence) and stop (cease) inputs of counter/timer **30**.

In operation of the slope A/D converter **10** of **FIG. 2**, switches **15** and **17** are closed initially, while at the same time switches **18** and **20** are open. Consequently, capacitor **12** is then connected between ground and the discharge reference voltage of source **23**. Sufficient time is allotted to allow the capacitor to charge (or discharge) so that the level of charge on the capacitor reaches the imprecise and non-critical value of the reference voltage, which may range from about 0.3 v to 0.5 v below the level of electrical ground, for example. This imprecise and non-critical value is a key point in the context of the present invention, in that it is only necessary to discharge the capacitor slightly below ground. Simultaneous with this charging (or discharging) of the capacitor, the A/D counter/timer **30** is reset to zero. During these events, comparators **26** and **27** are held inactive.

When the charge on capacitor **12** reaches the discharge reference voltage level, switches **15** and **17** are opened, and, an instant of time later, switches **18** and **20** are closed. The timing of the switch transitions is such that switches **15** and **17** are never closed at the same time as switches **18** and **20** are closed. Now the capacitor begins charging by virtue of current flow from constant current source **11**, commencing from the level of the discharge reference voltage of source **23** just below ground to a predetermined voltage level exceeding the highest level anticipated for any instantaneous sample voltage of the analog input signal to

comparator **27**.

When the charge on capacitor **12** reaches or barely exceeds the level of electrical ground (0), comparator **26** responds by transitioning low to cause A/D counter/timer **30** to commence its count. Capacitor **12** continues charging and, when its voltage level reaches or barely exceeds the sampled voltage level of the analog input signal to comparator **27**, the latter comparator responds by transitioning low to cause A/D counter/timer **30** to cease counting.

The A/D result may now simply be read -- or otherwise taken and used, for example as an input to a microcontroller with which the converter is associated -- from the capture register(s) of A/D counter/timer **30**. An accurate digital value representative of the analog input to the converter is obtained without need for additional program memory or a multiplicity of computation cycles as have characterized prior art converters. In the circuit of the present invention, the start of the A/D conversion is always triggered at the zero (ground)-crossing point. It is immaterial whether dielectric absorption maintains some residual charge on the capacitor, because the transitioning of comparator **26** and the commencement of the count occurs at the precise time that the voltage level on the capacitor crosses ground level, and that operation takes place for each conversion.

Further, the conversion is independent of any delay that may be experienced in turning on the constant current source, because that source is already operating upon (and indeed, is ultimately responsible for) occurrence of the comparator transition to commence the count. In addition, conversion throughput is increased by virtue of a faster computation of the digital conversion value than has

been achievable by prior art techniques. After the A/D conversion result is read from the capture register **30**, capacitor **12** is discharged by closing switches **17** and **20** while **15** and **18** are left open. The overall operating sequence is then repeated for the next conversion.

This operation is further illustrated by reference to **FIGS. 3**, **4**, and **5**. **FIG. 3**, which is a timing diagram of voltage (Y-axis) versus time (X-axis) at various points in the sequence of operation of the slope A/D converter of **FIG. 2**, illustrates two exemplary cycles of conversions of the analog input voltage. The only difference between the two cycles is in the charge duration. Initially, the DSCHG signal (see **FIG. 4**, a more detailed diagram of the converter) is active, and the CHG signal is inactive. The CAP1 node of capacitor **12** is grounded, and the CAP2 node of the capacitor is allowed to charge to the discharge reference voltage (i.e., a level at least slightly below analog ground, 0.5 v in this example) through switches **15** and **17**. Next, the DSCHG signal is deasserted (once allowing the capacitor to fully charge), and a short time later the CHG signal is asserted which grounds the CAP2 capacitor node through switch **20** and connects the CAP1 capacitor node to the constant current source through switch **18** (not shown in **FIG. 4**). Because the capacitor polarity has been reversed, the CAP1 node is -0.5V with respect to ground at this time. Subsequently, the CAP1 capacitor node begins charging from the constant current source.

When the capacitor voltage reaches or slightly exceeds analog ground, the comparator **26** trips low, which starts the A/D timer used in the slope conversion, as indicated by the NSTART signal in **FIG. 3**. The capacitor continues

to charge while the timer is running, until the capacitor voltage reaches or slightly exceeds the analog input level. At that time, comparator **27** switches low, stopping the A/D timer as indicated by the NSTOP signal in **FIG. 3**. The capacitor may continue to be charged until the DSCHG signal is re-activated or the current source reaches its compliance limit, whichever occurs first, but without adding to the content of the A/D timer. The user then reads or otherwise uses the contents of the A/D timer for the result of the conversion. At this point the capacitor is discharged (to a voltage level at least slightly below the analog ground level), and the sequence is repeated for each conversion cycle.

In **FIGS. 3** and **4**, A_{IN} is the analog input voltage to be converted to a digital value, and V_{REF} is the discharge reference voltage. **FIG. 5** is similar to the Cartesian coordinate plot of **FIG. 1** except that it now represents the results obtained with the embodiment of **FIGS. 2** and **4**. The zero count always occurs at zero volts, thereby substantially eliminating the error attributable to offset, and the dielectric absorption effects and turn-on delay effects are minimized.

It will be observed that the slope A/D conversion method of the invention converts an instantaneous analog value measurement to an accurate digital representation in a manner akin to initially storing a packet of energy of magnitude just below analog zero in a substantially depleted energy storage means, gradually adding a second packet of energy to the energy storage means to increase its stored energy to a level not only exceeding the predetermined reference energy level but ultimately exceeding the highest value which is anticipated for the analog input, and counting the increments of time starting with achievement of analog zero level in the

energy storage means and ending with achievement of the then-current level of the instantaneous analog input in the energy storage means, as a digital value representative of that instantaneous analog input level. In response to cessation of the timed count, the energy storage means is again depleted in preparation for a new analog-to-digital conversion.

An alternative embodiment of a slope A/D converter **10'** according to the present invention is shown in block diagrammatic form in **FIG. 6**. In this alternative embodiment, means are provided for converting the bandgap reference simultaneously with converting the analog input. As in the embodiment of **FIG. 2**, the circuit **10'** includes a constant current source **11'**, a capacitor **12'**, a plurality of switches **15'**, **17'**, **18'**, and **20'**, a discharge reference voltage source **23'**, a pair of comparators **26'** and **27'**, and an A/D timer/capture register **30'**.

The embodiment of **FIG. 6**, however, additionally includes a second A/D timer/capture register **40**, and a comparator **42**. The operation of this alternative embodiment is substantially identical to that of the preferred slope A/D converter embodiment of **FIG. 2**, except that the count of A/D timer/counter **40** is commenced simultaneously with the count of A/D timer/counter **30'** owing to the parallel connection of the same (start count) input of each of the two to the output of comparator **26'**. Additionally, the count of timer/counter **40** is stopped when the charge on capacitor **12'** at one input of comparator **42** barely exceeds the bandgap reference voltage applied as the other input of the latter comparator.

FIG. 7 illustrates the use of the slope A/D converter of **FIG. 2** (or of **FIG. 6**) of the present invention in or in conjunction with a microcontroller **50**

which is used to control one or more parameters of an external system, such as the temperature within an enclosure. The enclosure temperature is monitored and converted to the analog input voltage to the A/D converter, and the A/D conversion is used to allow the microcontroller to control the operation of a heating or cooling system to accurately maintain the enclosure temperature at a preset value.

Although certain preferred embodiments and methods are described herein, persons skilled in the art will recognize from the foregoing description that variations and modifications of the described embodiments and methods may be made without departing from the true spirit and scope of the invention. For example, the constant current source may be replaced by any device capable of delivering charge to the capacitor at a constant rate, to assure that the count, or the timed interval itself, is a digital value accurately representing the then-current analog input voltage. Also, although a capacitor is the preferred energy storage means, it could be replaced with some other device for storing electrical energy that will not suffer substantial leakage during the period the time interval is measured. Accordingly, it is intended that the invention shall be limited only to the extent required by the appended claims and the rules and principles of applicable law.

What is claimed is:

1. A slope analog-to-digital (A/D) converter, comprising:

capacitor means for storing voltage;

reference means for selectively placing said capacitor means at a preselected reference voltage level below electrical ground level;

constant current source means for selectively charging said capacitor means from said reference voltage level below ground level toward a predetermined voltage level above ground level and exceeding an anticipated highest level of an analog input signal to the converter;

first comparator means responsive to said capacitor means first reaching a charge at or slightly exceeding ground level during said selective charging for initiating commencement of a timed count;

second comparator means responsive to said capacitor means first reaching a charge at or slightly exceeding the then-current actual level of said analog input signal to the converter but below said predetermined voltage level, for initiating cessation of the timed count; and

register means for storing a digital conversion value equivalent to the count reached between commencement and cessation of the timed count, and thereby constituting the digital value representative of the then-current actual level of said analog input signal.

2. The slope A/D converter of claim 1, further including:

means responsive to cessation of the timed count for discharging said capacitor means in preparation for a new analog-to-digital conversion.

3. The slope A/D converter of claim 1, wherein said preselected reference voltage level is imprecise.

4. A device for controlling a parameter of an external system, using analog-to-digital (A/D) conversion of sampled values of the magnitude of a variable analog input voltage derived from the parameter to be controlled, comprising:

a capacitor for storing voltage;

means for selectively delivering electrical charge to the capacitor at a constant rate for storage of voltage in said capacitor according to the level of charge delivered thereto over an interval of time;

means for causing said charge delivering means to place a voltage on said capacitor below a predetermined reference level, and for then increasing the voltage stored on said capacitor until it exceeds the magnitude of the current sample of the analog input voltage;

means for timing the interval between the point at which the increasing voltage on the capacitor reaches said predetermined reference level, and the point at which said increasing voltage reaches the magnitude of said current sample of the analog input voltage; and

means for using said timed interval as a digital measure of the value of the magnitude of said current sample of the analog input voltage.

5. The device of claim 4, further including:

means responsive to the cessation of said timed interval for discharging said capacitor in preparation for converting the next sampled value of the analog input voltage.

6. The device of claim 5, wherein:

said predetermined reference level of the voltage stored on the capacitor is not a precisely regulated value but may lie anywhere in a predetermined range of values without adversely affecting the accuracy of the A/D conversion of the current sample of said analog input voltage.

7. The device of claim 6, further including:

means for using the timed interval to control said parameter of the external system.

8. The device of claim 6, wherein:

said timing means includes means for counting fixed increments of time from said point at which the increasing voltage on the capacitor reaches said predetermined reference level to said point at which the increasing voltage reaches the magnitude of said current sample of the analog input voltage, the cumulative

count between the two points constituting said digital measure of the analog input voltage.

9. The device of claim **6**, wherein:

said means for delivering electrical charge includes a constant current source.

10. A method of converting an instantaneous value of a variable analog input voltage to a digital value representative thereof, which comprises the steps of:

discharging a capacitor until the level of the voltage stored therein is at least slightly below the level of an electrical ground reference;

charging the capacitor at a substantially constant rate toward a level of stored voltage that exceeds the magnitude of the anticipated highest value of the analog input voltage;

counting increments of time starting with the moment at which the level of the voltage stored on the capacitor as a result of the charging reaches ground reference level and ending with the moment at which the level of the voltage stored on the capacitor as a result of the charging reaches the current magnitude of the analog input voltage; and

using the cumulative count as the digital value corresponding to the value of the analog input voltage at the time the count ended.

11. The method of claim **10**, including:

performing the step of discharging said capacitor after reaching said cumulative count, in preparation for the next analog-to-digital conversion of the instantaneous value of the analog input voltage.

12. The method of claim **10**, wherein:

the step of discharging the capacitor is performed without concern for the precise level of the stored voltage therein relative to the level of electrical ground, but only that the former is at least slightly less than the latter.

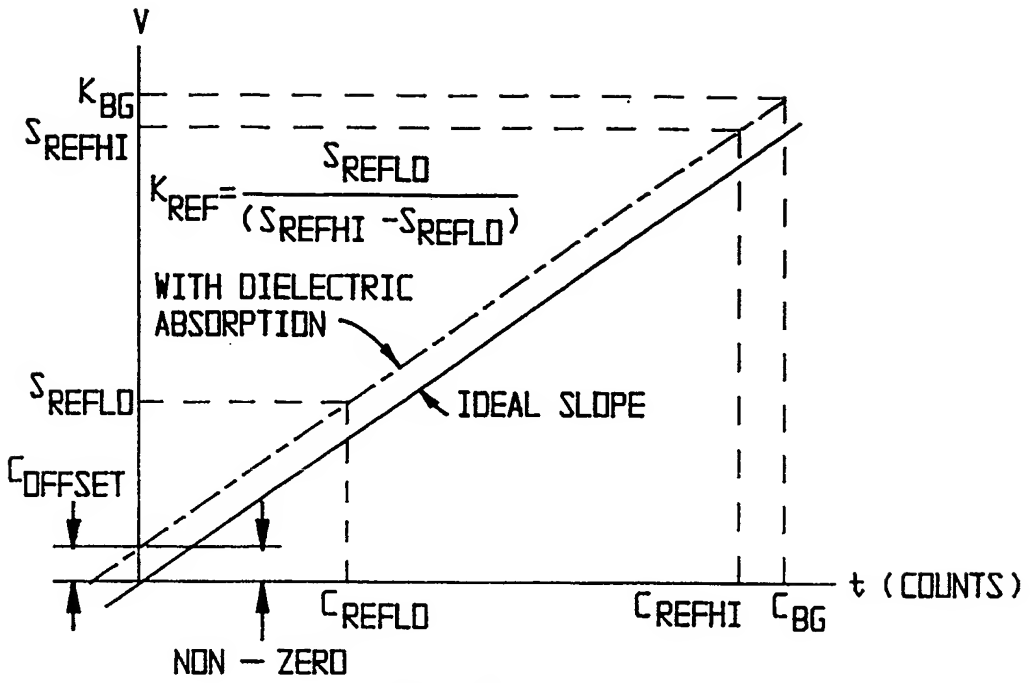
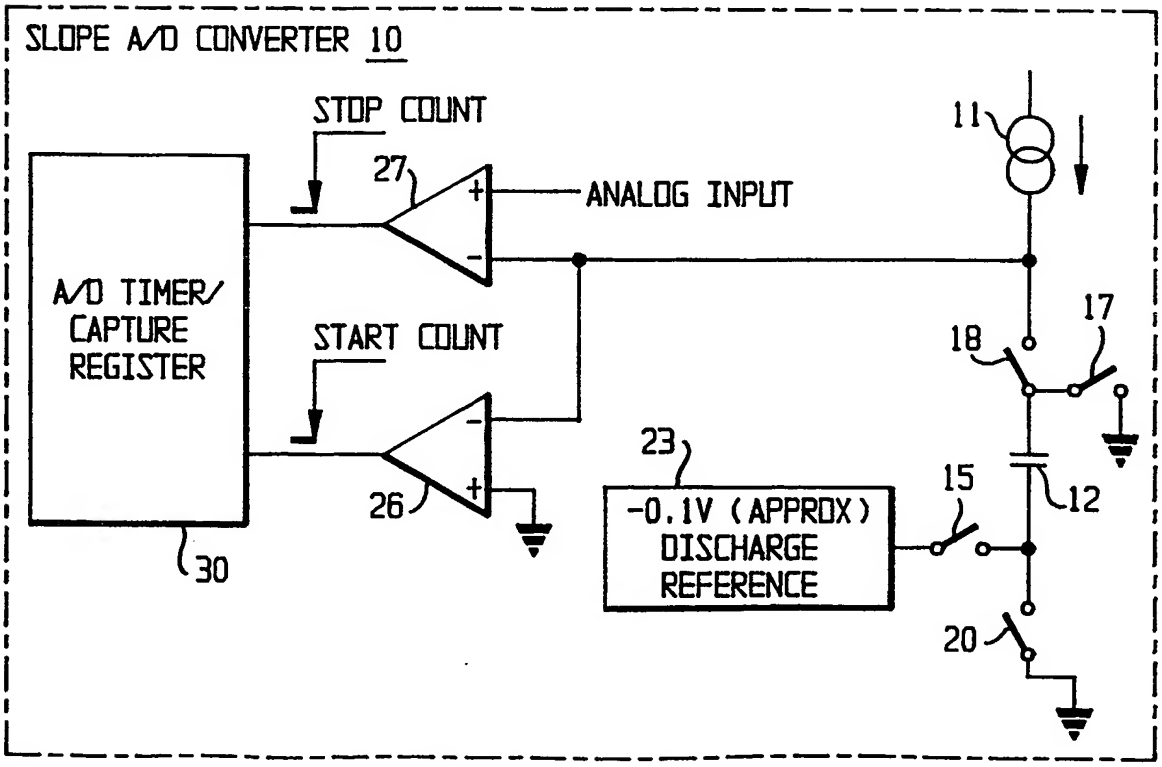


FIG. 1 (PRIOR ART)

FIG. 2



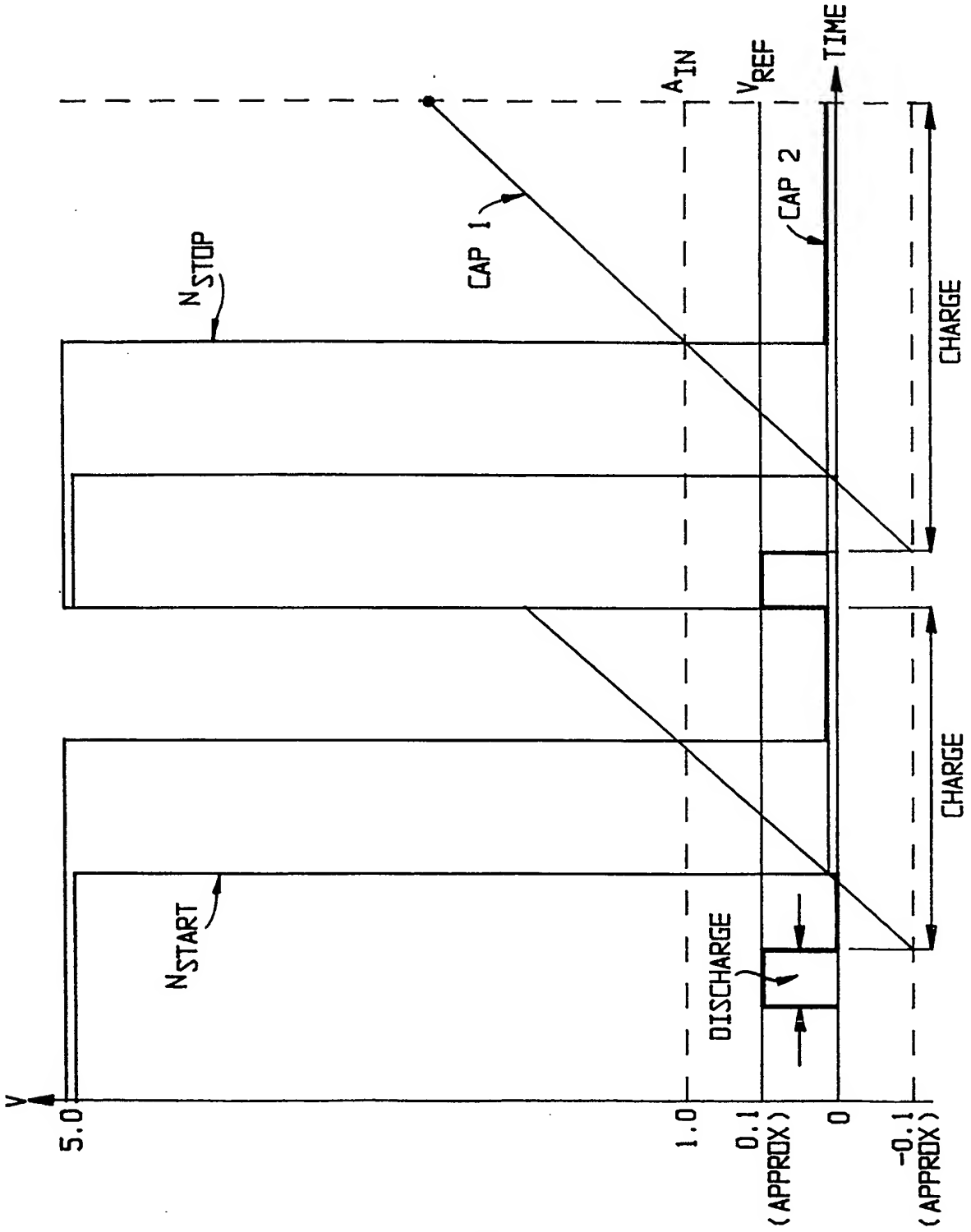

V
5.0
1.0
0.1
(APPROX)
0
-0.1
(APPROX)
N_{START}
N_{STOP}
DISCHARGE
CAP 1
CAP 2
CHARGE
CHARGE
A_{IN}
V_{REF}
TIME

FIG.3

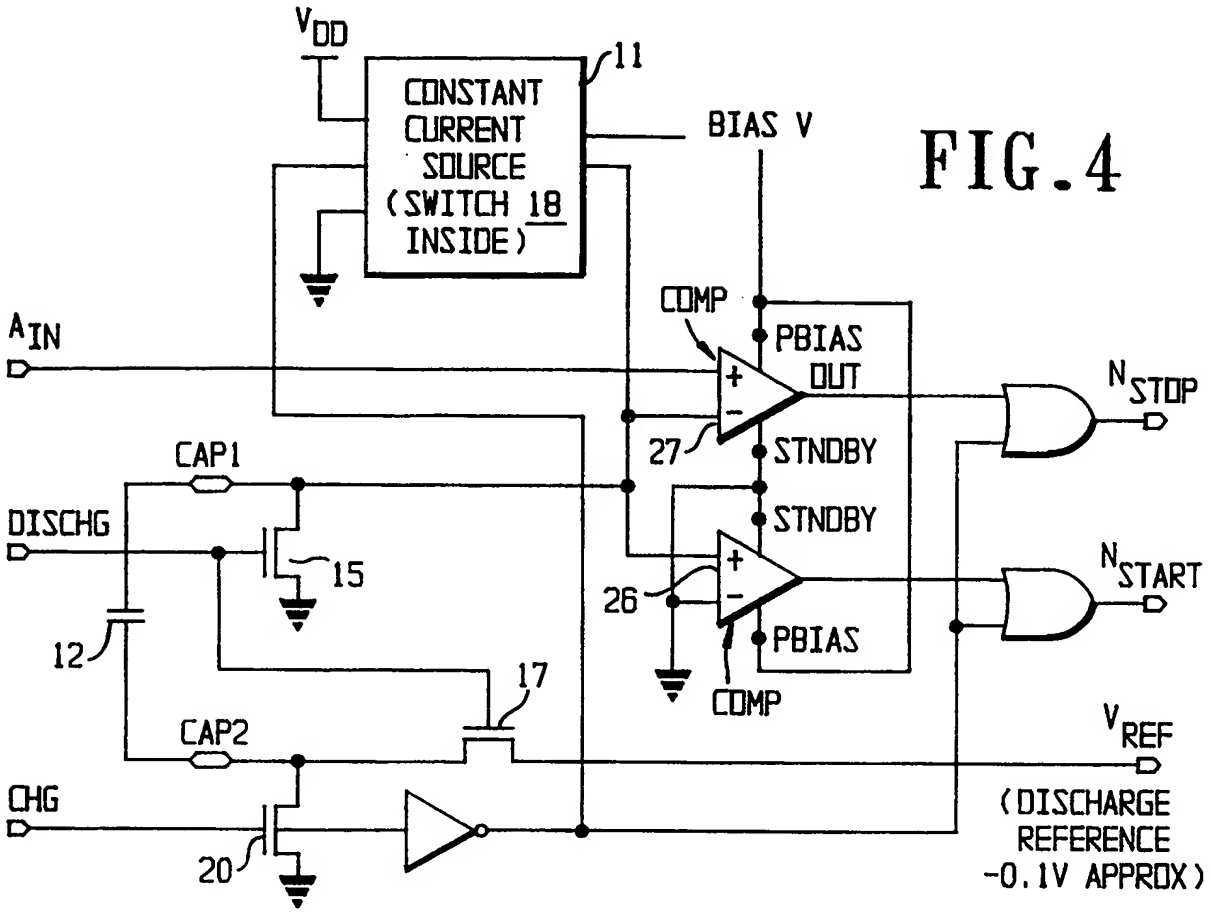

V_{DD}
CONSTANT CURRENT SOURCE (SWITCH 18 INSIDE)
11
BIAS V
A_{IN}
COMP
PBIAS OUT
N_{STOP}
27
STNDBY
CAP1
DISCHG
STNDBY
15
N_{START}
26
12
17
PBIAS
COMP
CAP2
V_{REF}
CHG
(DISCHARGE REFERENCE -0.1V APPROX)
20

FIG.4

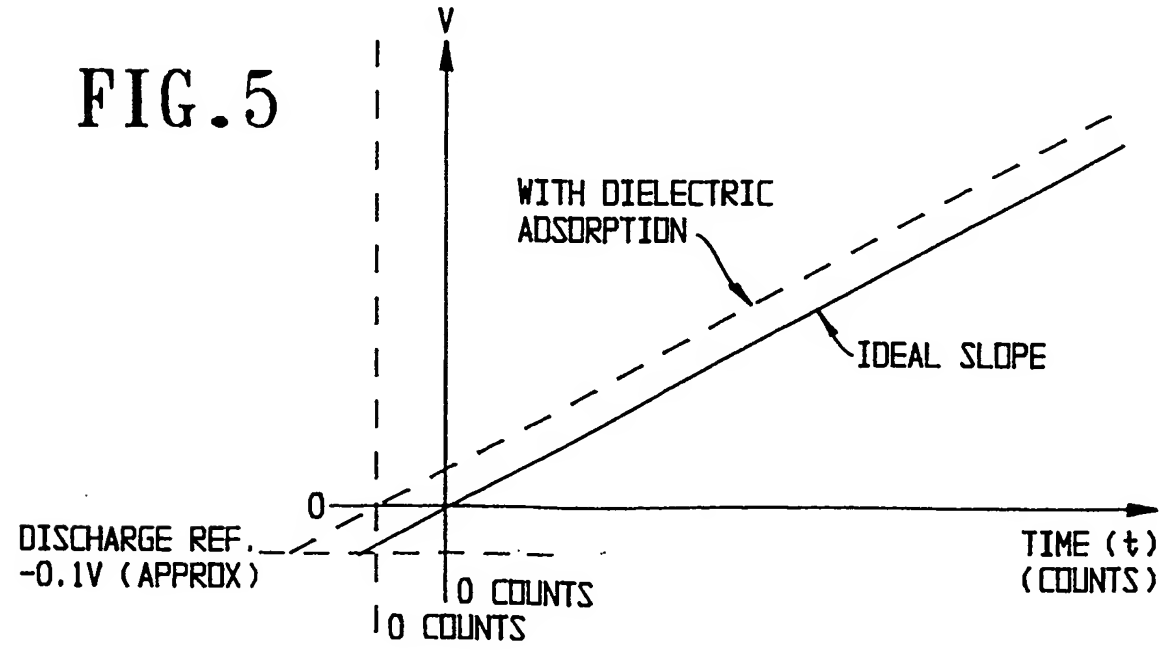

V
WITH DIELECTRIC ADSORPTION
IDEAL SLOPE
0
DISCHARGE REF. -0.1V (APPROX)
TIME (t) (COUNTS)
0 COUNTS
0 COUNTS

FIG.5

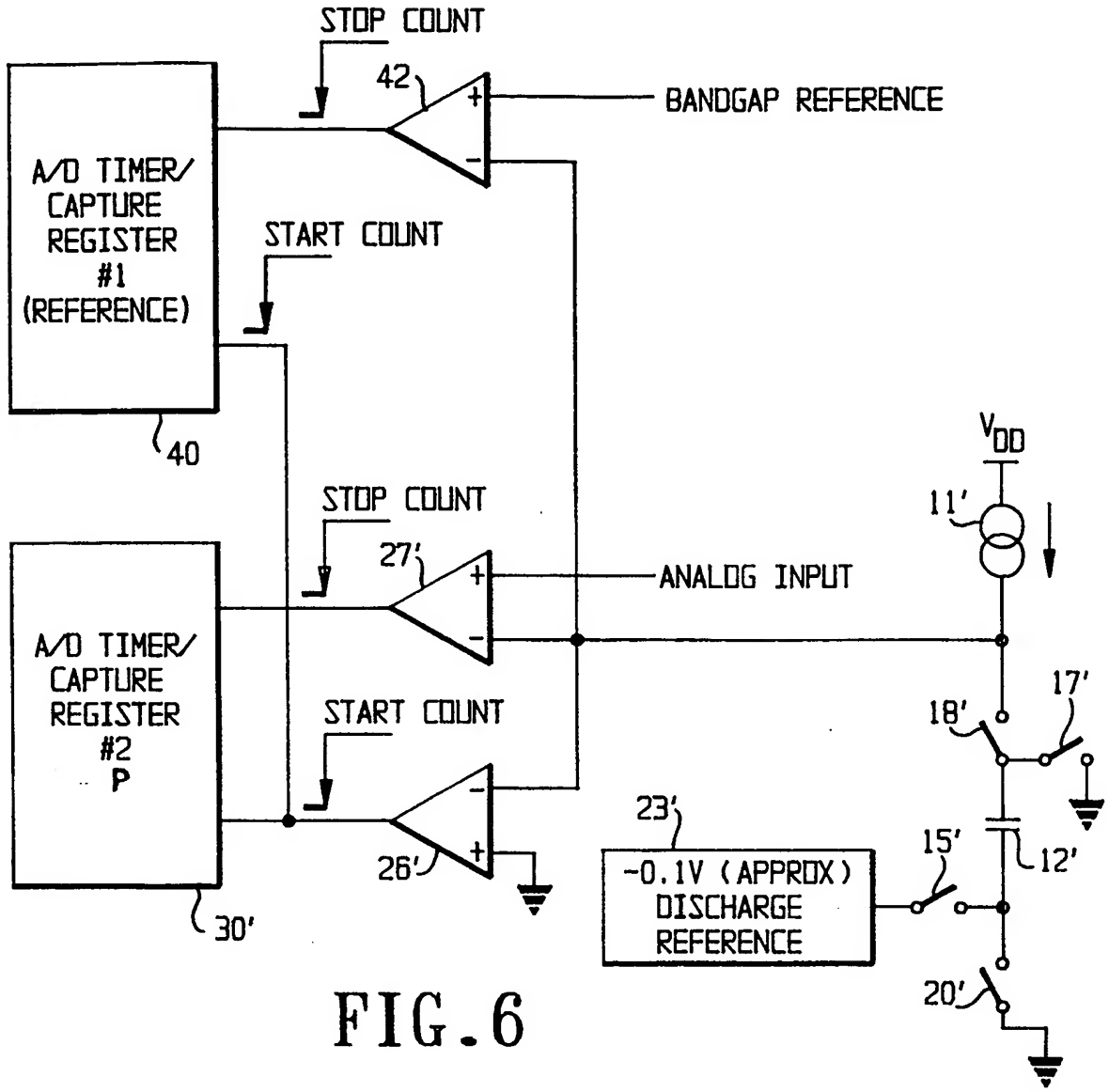

STOP COUNT
42
BANDGAP REFERENCE
A/D TIMER/ CAPTURE REGISTER #1 (REFERENCE)
START COUNT
40
STOP COUNT
27'
ANALOG INPUT
A/D TIMER/ CAPTURE REGISTER #2 P
START COUNT
26'
30'
V_{DD}
11'
17'
18'
23'
15'
12'
-0.1V (APPROX) DISCHARGE REFERENCE
20'

FIG.6

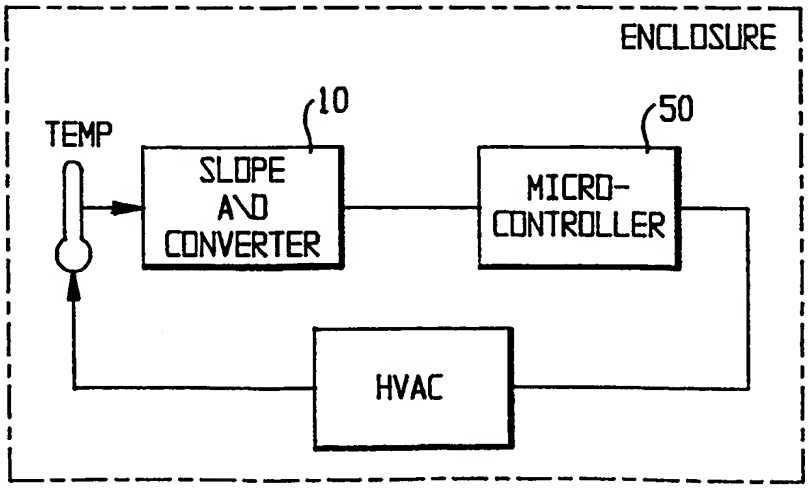

ENCLOSURE
TEMP
10
SLOPE A\D CONVERTER
50
MICRO-CONTROLLER
HVAC

FIG.7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/21326

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H03M 1/56
US CL :341/169
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 341/169, 164, 165, 166

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,127,810 A (PURLAND) 28 November 1978 (28.11.78), see the abstract, col. 2, line 51 through col. 3, line 32.	1-12
Y	US 3,613,112 A (KANTER) 12 October 1971 (12.10.71), see col. 6, lines 61-64.	1-12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
07 JANUARY 1998

Date of mailing of the international search report
23 FEB 1998

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